CLAIMS

1. A transceiver of a transmission system having a device for producing a chirp signal, wherein there is provided a memory (RAM, ROM) in which is stored a plurality of different chirp sequences which respectively correspond individually or in pairs to a predetermined chirp signal, wherein upon call a desired individual chirp sequence or a pair of chirp sequences is read out of the memory and a predetermined chirp signal is produced by means of the producing device which preferably singly or in pairs has the combination of a digital/analogue converter and a low pass member.

2. A transceiver as set forth in claim 1 characterised in that the chirp sequences stored in the memory can be sampled and bit-quantized chirp signals in the baseband, in the original frequency position or in the IF position, wherein bit quantization can be freely selected in the range of 1...n.

3. A transceiver as set forth in claim 2 characterised in that the chirp signal (which can be any one) can be produced without a corresponding chirp filter, wherein outputted at the output of the producing device are two signals I and Q which correspond to the real part and the imaginary part of the predetermined chirp signal in the baseband.

4. A transceiver as set forth in claim 2 wherein outputted at the output of the producing device is a signal which corresponds to the predetermined chirp signal in the transmission frequency position.

5. A transceiver as set forth in claim 2 wherein outputted at the output of the producing device is a signal which corresponds to the predetermined chirp signal in the intermediate frequency position.

6. A transceiver as set forth in claim 2 characterised in that for data transmission convolution pulses, that is to say combination signals

comprise upchirp pulses and downchirp pulses, are used, this involving purely real signals so that only one single chirp sequence has to be stored in the memory for the representation thereof in the baseband.

7. A transceiver as set forth in claim 3 wherein the output signals I and Q of the producing device are converted into the transmission frequency band by means of an I/Q modulator.

8. A transceiver as set forth in claim 5 wherein the output signal of the producing device is converted from the IF position into the transmission band by means of a modulation device (for example a mixer, a modulator or a simple multiplier).

9. A transceiver as set forth in claim 6 wherein the convolution pulse baseband signal at the output of the producing device is impressed on a real carrier signal by means of a single modulation member (for example a mixer, a modulator or a simple multiplier) and thereby converted into the transmission frequency band.

10. A transceiver as set forth in one of claims 1 through 5 wherein chirp signals of a differing BT-product and/or a differing time-frequency characteristic are stored in the memory and can be called up therefrom.

11. A transceiver as set forth in claim 10 characterised in that it is possible to have recourse to different ones of the stored chirp sequences in dependence on the transmission requirements.

12. A transceiver as set forth in claim 10 wherein switching-over to other chirp sequences can take place during ongoing transmission.

13. A transceiver as set forth in claim 1 characterised in that the required chirp sequences in a process of starting up operation or

initialisation are transferred into the memory of the transceiver by download and if required can also be replaced by re-programming.

14. A transceiver as set forth in claim 2 wherein the sampled chirp signals are additionally weighted with selectable filter functions (for example with a cosine roll-off characteristic) prior to quantization and storage in the memory.

15. A transceiver as set forth in one of the preceding claims wherein the chirp signals which come in at the receiver end are compressed with suitable dispersive filters in the carrier frequency band and are then directly and asynchronously demodulated into the baseband.

16. A transceiver as set forth in one of the preceding claims wherein the chirp signals coming in at the receiver end are firstly converted into the intermediate frequency position, then compressed with suitable dispersive filters into the IF position and then asynchronously demodulated into the baseband.

17. A transceiver as set forth in one of the preceding claims wherein the receiver device can be tuned (= programmed) to the chirp signal used at the transmitter end by simple exchange of the dispersive filters used while retaining all other receiver components.

18. A transceiver, in particular as set forth in one of the preceding claims, for producing, emitting and receiving convolution signals, wherein the convolution signals are compressed at the receiver end in the carrier frequency position by means of complementary dispersive delay lines and demodulated directly and asynchronously into the baseband by multiplication of the output signals of both delay lines.

19. A transceiver as set forth in one of the preceding claims, for producing, emitting and receiving convolution signals, wherein the

convolution signals are firstly converted at the receiver end into the intermediate frequency position, compressed by means of complementary dispersive delay lines and demodulated asynchronously into the baseband by multiplication of the output signals of both delay lines.

20. A transceiver as set forth in claim 19 wherein the congruence in respect of time of the envelope curves of the two compressed signals is used as a criterion for coincidence of the IF center frequency and the center frequency of the complementary dispersive filters in order to tune the local oscillator of the receiving device in a phase regulating circuit.

21. A transceiver as set forth in claim 19 wherein the output signals of the complementary dispersive delay lines are firstly passed to an envelope curve detector with subsequent threshold value comparator and the output signals of the threshold value comparators are passed to a phase detector whose output signal reflects the displacement in respect of time of the two envelope curves in respect of amount and polarity.

22. A transceiver as set forth in claim 21 wherein the output signal of the phase detector is passed to a regulator which changes the setting voltage of a voltage-controlled oscillator (VCO) for producing the local oscillator (LO) at the receiver end, until both envelope curves are congruent.

23. A transceiver as set forth in one of the preceding claims characterised in that the received signal is synchronised to the center frequency of the complementary dispersive group transit time filters.

24. A transceiver as set forth in one of the preceding claims characterised in that the phase regulating circuit also regulates out changes in the center frequency of the dispersive filters, which were produced by a rise in temperature, ageing or other influences.

25. A transceiver as set forth in one of the preceding claims for burst-wise transmission of data sequences by means of convolution pulses, wherein a data sequence to be transmitted is preceded by a preamble comprising convolution pulses, which serves specifically for bringing frequency regulation into effect.

26. A transceiver as set forth in claim 25 wherein upon the attainment of the steady-state condition of frequency regulation the VCO setting voltage is sampled with a sample-and-hold member and is held fast for the duration of a data burst.

27. A transceiver as set forth in one of the preceding claims for burst-wise transmission of upchirp/downchirp pulses, wherein a data sequence to be transmitted is preceded by a preamble comprising convolution pulses, which serves specifically for bringing frequency regulation into effect and upon the attainment of the steady-state condition of frequency regulation the VCO setting voltage is sampled with a sample-and-hold member and is held fast for the duration of a data burst.

28. A transceiver as set forth in one of the preceding claims for automatic frequency regulation in a system for burst-wise transmission of upchirp/downchirp pulses, wherein a data sequence is preceded in a preamble by a series of mutually alternate upchirp and downchirp pulses and the phase regulating circuit as shown in Figure 3 regulates not to a condition of congruence of the envelope curves but to a phase displacement of 180° and upon the attainment of the steady-state condition of frequency regulation the VCO setting voltage is sampled with a sample-and-hold member and is held fast for the duration of a data burst.

29. A transceiver as set forth in claim 28 wherein the phase detector is adapted to be switched over for receiving convolution pulses or upchirp/downchirp pulses.

30. A transceiver as set forth in one of the preceding claims with frequency regulation for receiving upchirp/downchirp pulses, wherein an uninterrupted sequence of symbols which is the same as the detected symbols of a convolution pulse sequence is produced in both branches which adjoin the dispersive filters by the insertion of dummy symbols so that a subsequent phase detector can effect checking in respect of congruence of the envelope curves and the regulating circuit shown in Figure 4 can also be used for frequency regulation of an upchirp/downchirp system.

31. A transceiver as set forth in claim 30 wherein the symbol sequences produced at the transmitter end are suitably scrambled prior to transmission, with the aim that the number of successive symbols of the same polarity does not exceed a specified value.

32. A transceiver as set forth in one of the preceding claims wherein the chirp signals which are received in the receiver are firstly converted into the IF position, compressed in complementary dispersive delay lines, then demodulated into the baseband with envelope curve detectors and converted with threshold value comparators into digitally processible signals and a logic EXCLUSIVE OR gate is used for deriving the symbol clock, said gate linking the output signals of the threshold value detectors, while a JK flip-flop is used for representation of the current datum, the inputs J and K thereof being connected to the outputs of the threshold value detectors and the clock input thereof being actuated with the output signal of the EXCLUSIVE OR gate.

33. A transceiver as set forth in one of the preceding claims for receiving convolution pulses, wherein the chirp signals which are received in the receiver are firstly converted into the IF position and compressed in complementary dispersive delay lines and the output signals of the delay lines are multiplied together and the output signal of the multiplier is

subjected to full-wave rectification and then passed to a threshold value comparator, at the output of which there is the symbol clock.

34. A transceiver as set forth in one of the preceding claims for receiving convolution pulses, wherein the chirp signals received in the receiver are firstly converted into the IF position and compressed in complementary dispersive delay lines, then demodulated into the baseband with envelope curve detectors and converted into digitally processible signals with threshold value comparators, and the outputs of the threshold value comparators are subjected to logical AND gating in order to derive the symbol clock.

35. A transceiver, in particular as set forth in one of the preceding claims for receiving convolution pulses, wherein the chirp signals received in the receiver are firstly converted into the IF position and compressed in complementary dispersive delay lines, and the output signals of the delay lines are multiplied together and the bipolar output signals of the multiplier are converted into digitally processible signals with subsequent threshold value comparators, whereupon the output signals of the threshold value comparators are subjected to logical AND gating in order to derive the symbol clock, while a JK flip-flop is used to represent the current datum, the inputs J and K of which are connected to the outputs of the threshold value detectors and the clock input of which is actuated with the output signal of the OR gate.

36. A transceiver with clock derivation as set forth in claims 32 - 35 having a gating device comprising a switch and a time control which operates in such a way that a symbol clock pulse entering at the input end is recognised by the time control and causes opening of the switch for the duration of a specified blocking interval which is shorter than a symbol clock period, whereby interference pulses which occur within the symbol interval are suppressed while the next following symbol clock pulse can again pass and can again trigger off the procedure.

37. A transceiver as set forth in claim 36 wherein a logic AND gate performs the function of the switch and a monoflop determines the length of the blocking interval.

38. A transceiver as set forth in claim 36 wherein the length of the blocking interval is variable and can be matched to the transmission situation, for example to interference phenomena on transmission.

39. A transceiver as set forth in claim 38 wherein a short blocking interval is used for the phase of bringing the receiving system into operation while the arrangement switches over to a longer blocking interval in the steady-state condition.

40. A transceiver as set forth in claim 36 wherein the gate, triggered by a symbol clock pulse, closes for the duration of a blocking interval, then opens for the duration of an opening interval (within which the next symbol clock pulse is expected) and then closes again for the duration of a blocking interval, and that process is continuously repeated.

41. A transceiver, in particular as set forth in one of the preceding claims, wherein the chirp signals received in the receiver are firstly converted into the IF position, compressed in complementary dispersive delay lines, and then the compressed signals are passed in both branches to a respective envelope curve detector, an average value detector and a peak value detector, wherein in downstream-connected threshold value comparators the output signal of the respective envelope curve detector is compared to a threshold value which can variably assume a value between the average value and the peak value of the detected signal.

42. A transceiver as set forth in claim 41 wherein in both branches the position of the threshold value can be digitally controlled between the signal average value and the signal peak value.

43. A transceiver as set forth in claim 42 wherein in both branches a voltage is added to the threshold value formed from the signal average value and the signal peak value, thereby providing that the threshold value at the comparator input is always higher than the noise amplitude at the output of the envelope curve detector.